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Substitute for Form 1449A/PTO				Complete If Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				Application Number:	TBD 10/603,711
(use as many sheets as necessary)				Filing Date:	Harcourt 6/25/03
				First Named Inventor:	Taylor R. Efland
				Group Art Unit:	TBD 2815
				Examiner Name:	Jasmine TBD Clark
				Attorney Docket No.:	TI-30963.1
Sheet	1	of	2		

**U.S. PATENT DOCUMENTS**

Exam. Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
AA	4,259,685			Romano	03/31/1981	
AB	4,518,982			DuBois, et al.	05/21/1985	
AC	5,610,442			Schnieder, et al.	03/11/1997	
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AG						
AH						
AI						
AJ						
AK						
AL						
AM						
AN						
AO						

**FOREIGN PATENT DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

		Complete If Known	
		Application Number	TBD
		Filing Date	Herewith
		First Named Inventor	Taylor R. Efland
		Group Art Unit	TBD 2818
		Examiner Name	Jasmine TBD Clark
Sheet	2	Attorney Docket No.	TI-30963.1

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
WJ	CA	"Controlled Collapse Reflow Chip Joining", L. F. Miller, IBM J. Res. Develop., Vol. 13, May 1969, pp. 239-250	
	CB	"Geometric Optimization of Controlled Collapse Interconnections", L.S. Goldman, IBM J. Res. Develop., Vol. 13, May 1969, pp. 251-265	
	CC	"Paramedic Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Sevgin Oktay, IBM J. Res. Develop., Vol. 13, May 1969, pp. 272-285	
	CD	"Reliability of Controlled Collapse Interconnections", K.C. Norris and A.H. Landzberg, IBM J. Res. Develop., Vol. 13, May 1969, pp. 266-271	
↓ Jasmine	CE	"SLT Device Metallurgy and Its Monolithic Extension", P.A. Totta and R.P. Sopher, IBM J. Res. Develop., Vol. 13, May 1969, pp. 226-238	
	CF	"Studies of the SLT Chip Terminal Metallurgy", B.S. Berry, and I. Ames, IBM J. Res. Develop., Vol. 13, May 1969, pp. 286-296	
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	CJ		
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Examiner Signature	Jasmine Clark	Date Considered	03/13/04
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